A Multi-Level Converter with a Floating Bridge for Open-Ended Winding Motor Drive Applications

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***Abstract*—This paper presents a dual three phase open end winding induction motor drive. The drive consists of a three phase induction machine with open stator phase windings and dual bridge inverter supplied from a single DC voltage source. To achieve multi-level output voltage waveforms a floating capacitor bank is used for the second of the dual bridges. The capacitor voltage is regulated using redundant switching states at half of the main dc link voltage. This particular voltage ratio (2:1) is used to create a multi-level output voltage waveform with three levels. A modified modulation scheme is used to improve the waveform quality of this dual inverter. This paper also compares the losses in dual inverter system in contrast with single sided three-level NPC converter. Finally, detailed simulation and experimental results are presented for the motor drive operating as an open loop v/f controlled motor drive and as a closed loop field oriented motor controller.**

***Index Terms*—Field oriented control, floating bridge, Open End Winding Induction Machine (OEWIM), space vector.**

I. INTRODUCTION

VARIOUS multi-level converter topologies have been proposed during the last two decades [1-4]. Several converter topologies have been investigated to achieve multi-level output voltage waveforms, among them the diode clamped [3], flying capacitor [5, 6] and cascaded [4] converters are commonly used. Multi-level converters have lower dv/dt and reduced harmonic distortion along with lower semiconductor switching device blocking voltage requirements, thus multi-level converters are advantageous in medium voltage, high power or low voltage, high frequency applications [7-9].

Among the cascade converters, dual two-level inverter topology has received attention due to the simplicity of the power stage and the arrangement's fault tolerant capacity [10, 11]. Traditional dual two-level inverter topologies use two standard three-phase inverters to achieve a multi-level voltage output. This topology does not have the neutral point fluctuations found in NPC converters, uses fewer capacitors than the flying capacitor topology and requires fewer isolated supplies than H-bridge converters [5, 12, 13].

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Furthermore dual inverters are more reliable, because in case of a failure in one converter the outputs of the converter can be short-circuited and the system can then operate as a standard single sided three phase inverter[14]. To achieve multi-level voltage waveforms and to cut the path of common mode current flow two isolated dc sources are used for traditional dual inverter topology, increasing the size and weight of the system. In this paper a dual two-level inverter is presented which reduces the size and weight of the system for an open end winding induction motor drive application. Dual inverter topologies have been considered in numerous papers for different applications. The traditional dual inverter topologies (using two isolated dc sources) has been analyzed [15-20], with different space vector modulation schemes used to generate the multi-level output voltage waveforms. A block diagram of a traditional open phase load and converters is shown in Fig. 1. It is possible to use a single supply for the dual inverters with a common mode elimination technique [15, 21, 22]. These topologies use specific switching combinations that produce equal common mode voltages which cancel at load terminals. A reduction in the number of voltage levels and lower dc bus voltage utilization are the main disadvantages of this variation of the topology.

A modulation technique to balance the power flow between the two inverters in a dual inverter system has also been proposed [23-27]. This topology still uses an isolation transformer; the size of this transformer can be reduced at the expense of reduced modulation index. The floating capacitor bridge topology along with a suitable control scheme to allow the supply of reactive power was introduced in [28]. Other authors [29, 30] have presented methods to compensate for supply voltage droop in order to keep the drive operational in constant power mode. This topology uses a floating capacitor bridge to offset the voltage droop in high speed machines.

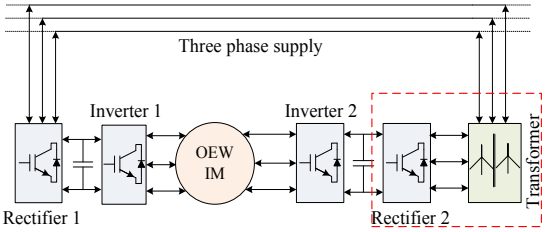

Fig. 1. Conventional open end winding IM drive topology.

In this paper, a circuit topology is analyzed which is used as a three-level open end winding induction motor drive. This topology uses dual inverters with only one DC voltage source at the primary side of the converter. The second

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bridge converter is connected to a floating capacitor bank. The aim of this topology is to eliminate the requirement for a bulky isolation transformer whilst achieving multi-level output voltage waveforms. The voltage across the floating capacitor bank is controlled using the redundant switching vectors along with a modified SVM scheme which avoids unwanted voltage levels in the phase voltage waveforms during the dead-time intervals, thus improving the overall waveform quality.

II. PROPOSED SYSTEM

A. Floating capacitor bridge inverter

The floating bridge capacitor dual inverter based topology has been analyzed for different applications [28, 31]. The topology can be used to supply reactive power to a machine and to compensate for any supply voltage droop [28, 32], but the possibility of multi-level output voltage waveforms were not considered. A control scheme to charge the floating capacitor bridge along with multi-level output voltage waveforms has been presented [33-35]. In this method the main converter works in six step mode and the floating converter is called conditioning inverter as it is improving the waveform quality.

The work described in this paper is to control the voltage across the floating inverter bridge capacitor using the redundant switching states, therefore removing the need for any isolation transformer and allowing the converter to achieve multi-level output voltage waveforms. Fig. 2 shows a block diagram of the dual inverter with a floating bridge and associated capacitor. The use of a dc link voltage ratio of 2:1 allows the dual bridge inverter to produce up to a three levels in the output voltage waveform [36, 37]. The power stage of the proposed topology is shown in Fig.3.

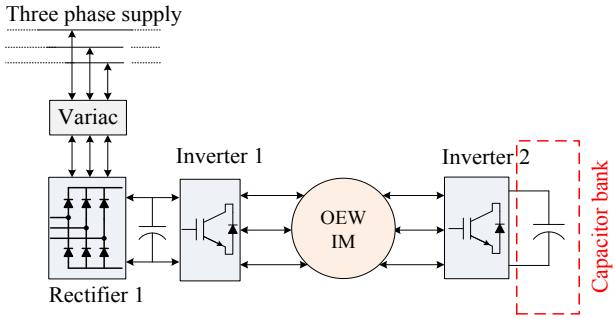

Fig. 2. Block diagram of proposed floating bridge topology.

B. Principles of operation

In order to show how the floating capacitor can be charged and discharged the possible switching states are analyzed. The space vector diagram for the topology is shown in Fig.4, which is derived by assuming that both converters as being supplied from isolated DC sources with a voltage ratio of 2:1. In Fig.4 the red numbered switching combinations discharge the floating capacitor, while the green numbered switching combinations charge the floating capacitor. The blue numbered switching combinations hold the last state of capacitor and are therefore neutral in terms of the state of charge of the floating capacitor. As an example state (74) shown in Fig.5 gives the switching sequences for both converter's top switches 7 (1 1 1) represents the top three switches for main inverter and 4 (0 1 1) represents the switching states for top three switches of the floating converter.

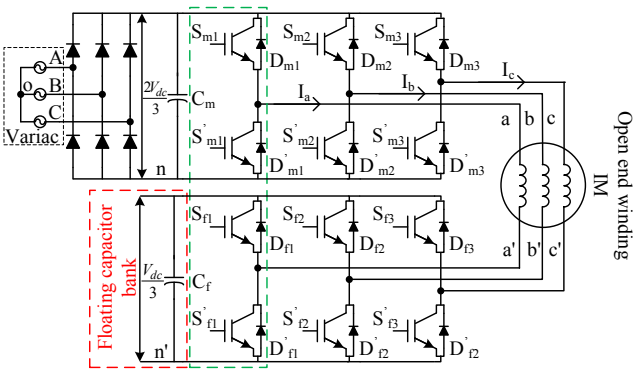

Fig. 3. Power stage of the floating bridge topology (the floating capacitor is charged to half of the main DC link voltage).

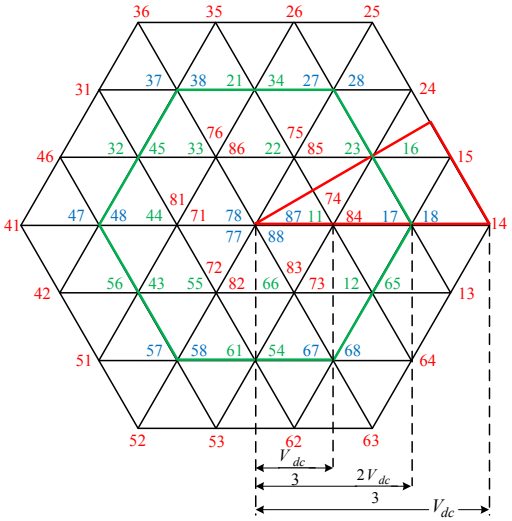

Fig. 4. Space vector of dual two-level inverter (source ratio 2:1).

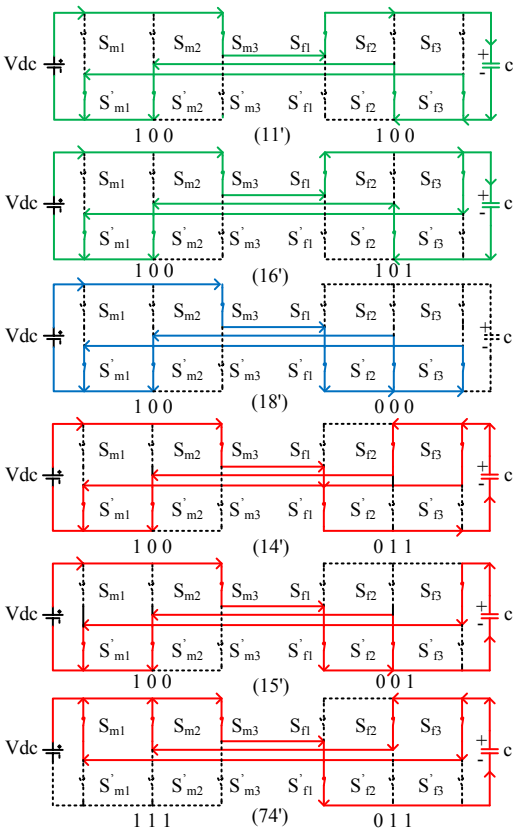

Fig. 5. Current flow for different switching state.

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It can be seen from the Fig. 5 that combinations (11) and (16) will direct the current through the positive to negative terminal of the floating capacitor thus will act to charge the capacitor. Combinations (14), (15) and (74) will result in a current in the other direction and will therefore act to discharge the capacitor. Combinations ending with 7 (111) or 8 (000) are zero states and will therefore have no impact of floating capacitor's voltage. It is evident from Fig. 4 that if the reference voltage is in outer hexagon then there are only two switching combinations in each sector to charge the floating capacitor. During inductive load operation capacitor discharge rate will be slower and will cause overcharging if the reference voltage lies in outer hexagon. Also, due to lack of charging states, the floating capacitor will discharge if the machine is drawing active power. To avoid these two phenomenon a restriction has to be imposed on modulation index. As a result the maximum useable number voltage levels across the load will be reduced to nine (thirteen for isolated sources) along with a slightly lower than ideal DC bus voltage utilization. Therefore the floating capacitor can charge to half of the main DC link capacitor voltage only if the modulation index (m) is limited as shown in equation (1).

$$m = 0.66 \tag{1}$$

This is 33% reduction of DC bus utilization in contrast with a dual inverter supplied by two isolated sources. The dual inverter with a zero sequence elimination technique also uses single supply with 15% reduction in DC bus utilization and can achieve five-level voltage across the load [21].

C. Modulation strategy

A decoupled space vector modulation strategy has been used for this dual inverter floating bridge topology. Switching combinations are selected in such a way that the average generated voltage for each of the converters is 180 degree phase shifted from the other [Fig.6 (a)]. These voltages will then add up at load terminal to match overall voltage reference [Fig.6 (b)]. Identification of the subsectors, dwell time calculation and the switching sequence design can be found in [38, 39].To achieve better results, the output switching sequences are modified. The modification of the pulses is necessary to minimize the unwanted voltage levels due to dead-time intervals in each phase leg [40, 41]. In general, the output voltage of a converter is governed by load current during dead-time intervals and the voltage is equal to one of the voltage levels before or after the dead-time intervals. The dual inverter with unequal voltage sources will show a different characteristic, instead of clamping the output voltage to one of the voltage levels before or after the dead-time interval voltage levels, it clamps the output voltage to some other voltage levels. This is true for simultaneous switching for each phase legs of the converters.

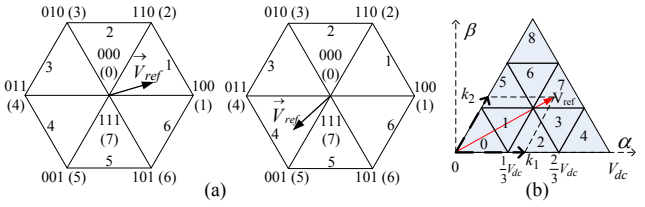

Fig. 6. (a) Space vector diagram of individual converter (not in scale). (b) Space vector diagram of the dual inverter system with sourece ratio of 2:1.

For an example, consider phase legs inside green dotted line in Fig. 3 for positive load current (current flowing from main to floating converter). If the top switches of the legs (S_{m1} & S_{f1}) are on then the load current will go through switch S_{m1} and diode D_{f1}. Now, if both legs go to its dead-time at the same time the load current will change direction and will go through diode D'_{m1} and diode D_{f1}. Finally when both the converter legs bottom switches (S'_{m1} & S'_{f1}) turned on current will go through diode $D'_{m1}$and switch S'_{f1}. It is clear that during dead-time interval, voltage level is different to the voltage levels before and after the dead-time interval. To avoid this unwanted voltage level, in this scenario, the main converter leg will go into its dead-time first and then second converter will go to its dead-time interval as soon as the main converter passes its dead-time interval. A generalized solution is shown in Fig. 7 for positive load current. It can be seen from the Fig. 7 that the pulses are delayed depending on the switching states transitions. Table I shows the generalized solution for positive and negative load currents to avoid the unwanted voltage levels.

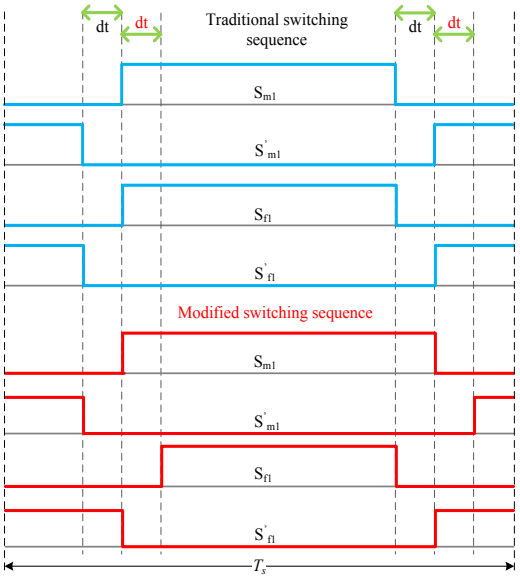

Fig. 7. Delayed dead-time intervals in both converters when current direction is positive.

Due to the modified switching sequences, the current direction does not change during the dead-time. The state of the floating capacitor will depend on the current just before the occurrence of dead-time interval. As an example, if the capacitor was charging then it will keep charging when the converter is in dead-time period. The value of dead-time is too small for the any overcharge or discharge to change the capacitor voltage drastically.

TABLE I

DELAY TIME DEPENDING ON CURRENT DIRECTION

	Inv-1 Top	Inv-1 Bot	Inv-2 Top	Inv-2 Bot
I > 0	Turn off	Turn on	Turn on	Turn off
I < 0	Turn on	Turn off	Turn off	Turn on

III. RESULTS

The proposed system has been simulated using PLECS and SIMULINK to compare losses between three different converter topologies shown in section III-A. Results from the converter operating as an open loop v/f motor drive are presented to show the converter operation. Finally results for a field oriented control for a closed loop motor drive are shown, the results are taken from the experimental setup is shown in Fig.8.

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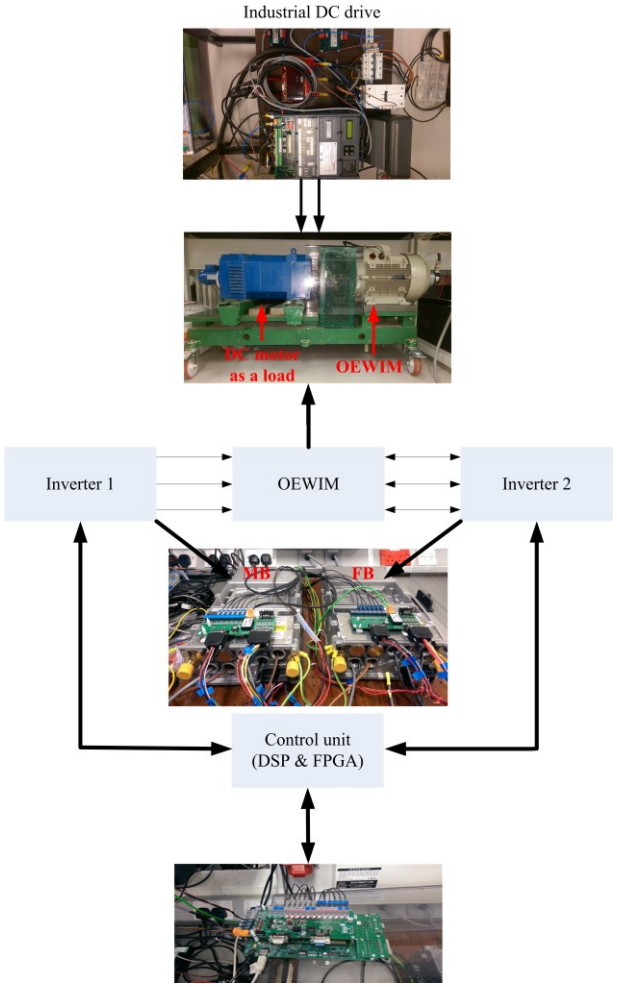

Fig. 8. Experimental converter setup.

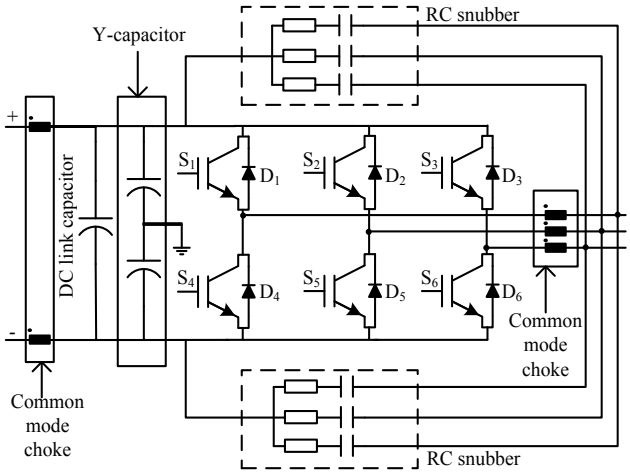

Fig. 9. Power stage of the experimental two-level converter.

The power converters used for this experiment was built using 'off the shelf' two-level converters. These two-level converters have R-C snubbers and common mode inductors. The converter also has onboard defined dead-time that varies from 4 – 4.1 µs along with propagation delay which varies from 0.1 to 0.2 µs, thus it is difficult to align the switching pulses accurately. A power stage diagram of the experimental two-level converter is shown in Fig.9. The parameters of the converter and machine are provided in table III. The control scheme was implemented using a DSP/FPGA based control platform. The capacitor of the floating bridge converter was chosen to have a sufficient ripple current rating for this experiment [3250 µF]. The converter is integrated with a 1250 µF film capacitor which has a 2000 µF electrolytic capacitor in parallel to minimize local ripple voltage.

A. Loss comparison

The losses of the proposed dual inverter system are compared in this section. Three converter types were selected, a single sided three-level NPC, a dual two-level inverter with equal DC link voltage ratio and the proposed dual inverter topology. All these three topologies provide three-level output voltages and therefore it is important to compare them in terms of losses. The losses were calculated for 12 kW drive used for experimental validation.

TABLE II

DEVICE VOLTAGE RATING COMPARISON

		Number of IGBT (voltage rating)	Number of diode (voltage rating)	Number of diodes in rectifier (voltage rating)	Capacitor Voltage
3-L NPC		12 (485 V)	18 (485 V)	6 (970 V)	485 V
Dual equal voltage		12 (485 V)	12 (485 V)	12 (485 V)	485 V
Dual Floating bridge	*Main*	6 (970 V)	6 (970 V)	6 (970 V)	970 V
	Float	6 (485 V)	6 (485 V)	n/a	485 V

The device losses were calculated using semiconductor device characteristics selected according to required blocking voltage and current requirements of the topology as presented in table II. The loss calculations were in terms of switching and conduction losses for the power converters and in this comparison all other circuit losses were ignored. Fig. 10 shows the efficiency at full load (12 KW) with varying switching frequency. It can be seen from the figure that, for this particular load, dual inverter with equal dc link voltage ratio has better efficiency than the other topologies. The three-level NPC has six extra clamping diodes, thus the losses are higher.

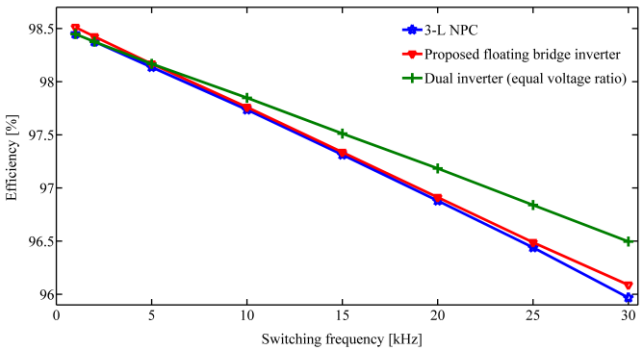

Fig. 10. Loss comparison in different power converter topologies.

The proposed floating bridge dual inverter has slightly better efficiency than three-level NPC but is less efficient than dual inverter with equal dc link voltage. The proposed floating bridge converter has two distinct switching patterns, one is for charging and the other is for discharging, thus it is difficult to maintain the minimum switch involvement for switching transitions. The reasons for using a dual inverter

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compared to single sided inverters are redundancy and to modulate high frequency fundamental. The traditional dual inverter topologies require isolated supply for both converters and thus increase the weight and size of the system. The proposed floating bridge topology eliminates the need for isolated supplies thus reduce the size and weight of the system.

B. Open loop v/f controlled IM drive

Results from the open loop v/f control of an open winding induction motor (one bridge floating) drive are presented in this section. To achieve experimental results main converter was supplied with a DC source of 500 Volts. The floating converter was maintained at half of the main DC link voltage and the switching frequency was set to 2 kHz. To demonstrate the steady state operation a demand reference frequency of 25 Hz was used. The reason for choosing this frequency is to maintain the *v/f* ratio for the machine which is rated at 690 Volts. To modulate this voltage the main converter needs to have a DC link voltage of 970 Volts. This was not achievable for the 'off the shelf' converters thus the rated speed was capped for this experiment. The results for open loop *v/f* controlled drive are presented from Fig. 11 to Fig. 12. Fig. 11 shows the no load voltage, current and floating DC link voltage, it can be seen that the drive charges the floating capacitor to required value and the converter achieves a multi-level output voltage waveform. To validate the open loop performance of an IM drive a step load was applied to the machine, shown in Fig. 12. It is evident from the figure that the capacitor can hold its charge during a sudden change in load and the effect on the capacitor voltage is minimal.

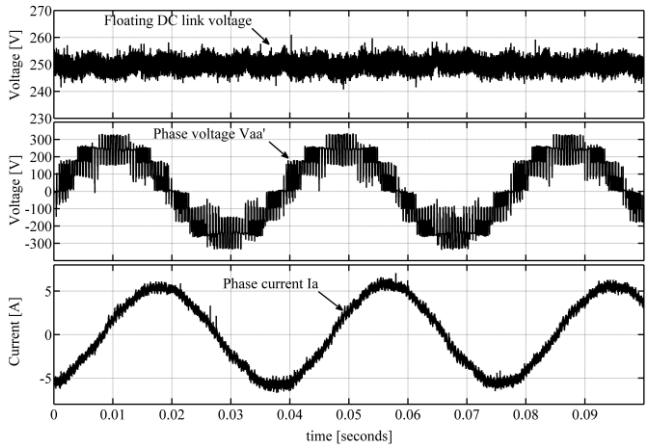

Fig. 11. Open loop v/f control IM drive Top to bottom : floating capacitor voltage, phase voltage $V_{aa'}$, and phase current I_a.

The results presented in Fig. 11 were achieved using the modified switching pulses to avoid unwanted voltage level during the dead-time interval. A magnification of the leg voltages and the phase voltage of the converters are shown in Fig. 13 with no modification to the gating pulses. It can be seen that the phase voltage is clamped to an unwanted voltage state for the duration of dead-time interval. The leg voltages and phase voltage is plotted in Fig.14 after the introduction of the modified switching pulses, showing that the leg voltages are changing state at the same time and spike duration is shorter. To ensure that the modification of the pulses is necessary for this topology the THD of load current and voltage was analyzed before and after the modified pulses were applied to the converters.

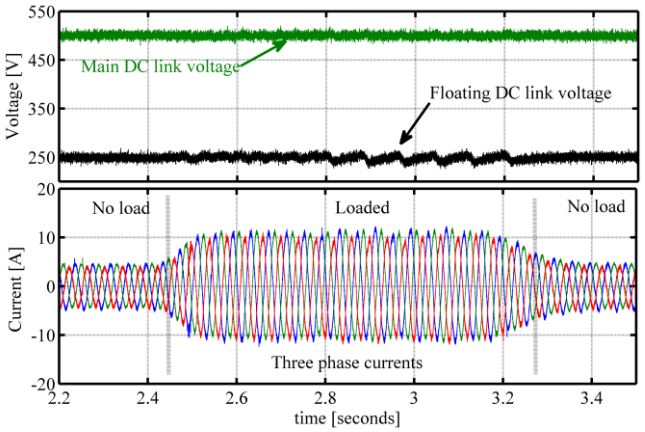

Fig. 12. Open loop v/f control IM drive Top to bottom : DC link voltages when an external load is applied to the machine and three phase currents.

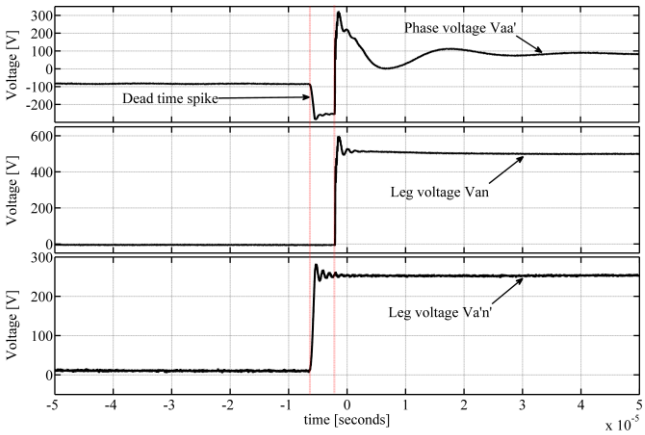

Fig. 13. Experimental results of voltages with traditional SVM pulses. Top to bottom: phase voltage $V_{aa'}$, Main inverter leg voltageV_{an} and floating inverter leg voltage $V_{a'n'}$.

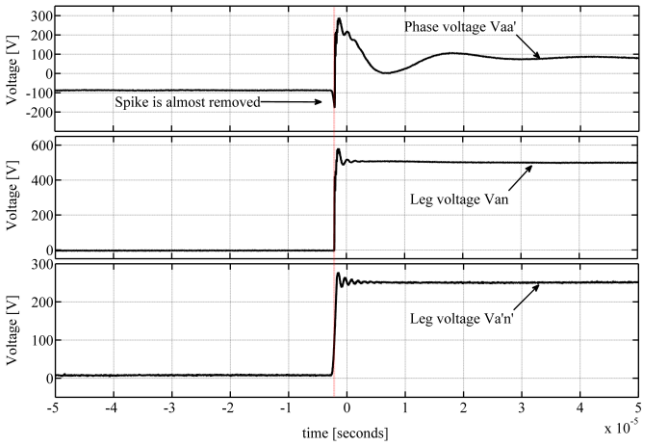

Fig. 14. Experimental results of voltages with modified gating pulses. Top to bottom: phase voltage $V_{aa'}$, Main inverter leg voltageV_{an} and floating inverter leg voltage $V_{a'n'}$.

The results are shown in Fig. 15 and Fig. 16, the current and voltage THD has reduced after the modified pulses were implemented. The difference between modified and non-modified pulses decreases with the increase of modulation index. Decrement of the THD differences are due to utilizing less number of dead-time spike producing switching combinations. The phase voltages also show oscillations after changing states; the oscillations can be seen Fig. 13 and Fig.14.

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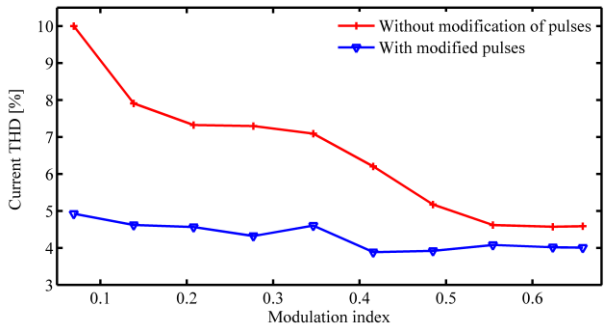

Fig. 15. Current harmonic distortion.

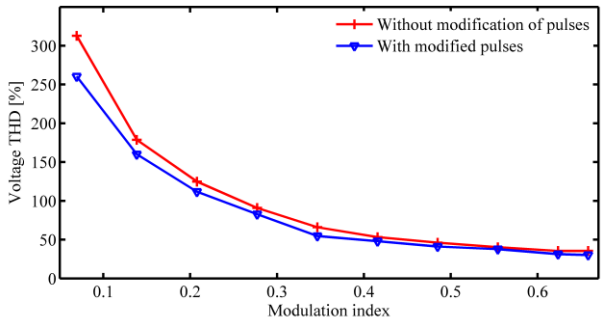

Fig. 16. Voltage harmonic distortion.

The frequency of the oscillation is near 35 kHz and is due to the snubber capacitance forming a resonant circuit with load inductance.

C. IRFO based close loop control

It is important to demonstrate the performance of the proposed converter in a high performance field oriented controlled motor drive as this is the target application. To achieve the results the main inverter was supplied from a 500 Volt DC source. The aim of the floating capacitor voltage control was to charge the floating bridge capacitor to half of the main DC link voltage. An indirect rotor flux orientation based control was implemented to decouple the flux and torque producing current of the induction machine. The floating capacitor was initially charged using reference d-axis 'field producing' current. After the floating capacitor was charged the speed command was set. An external load was applied by running the DC motor in torque control mode (braking) and results were taken to see the effect on floating capacitor voltage. A simplified block diagram of the field oriented control system is presented in Fig. 17. The block 'condition' is the protection algorithm to monitor the floating capacitor voltage. The algorithm compares the reference and actual floating capacitor voltage at the period of initial charging transient, the controller will shut down the system if capacitor voltage is more than 15% of reference voltage. The algorithm also protects the system after the speed command is set. The controller will shut down the system if the capacitor voltage deviation is more than +-15% of the demand value. A flow chart for this algorithm is shown in Fig. 18. Initial charging of the capacitor is presented in Fig. 19. To charge the capacitor initially, the machine was magnetized first. The amplitude of the magnetizing current reference i_d^* may not be the rated value. After magnetization process was done, a step reference voltage was applied to show the charging dynamics of floating capacitor. It can be seen from Fig. 19 that capacitor tracks the reference value and reaches steady state within 1.5 seconds.

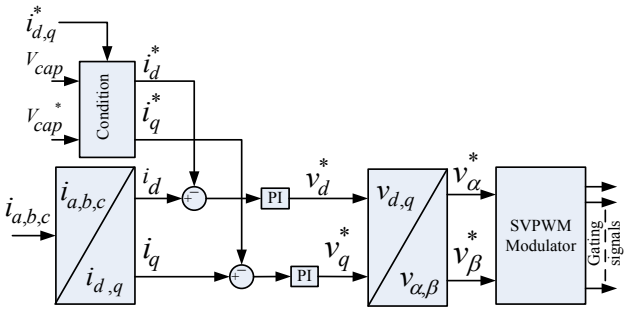

Fig. 17. Block diagram of vector control drive.

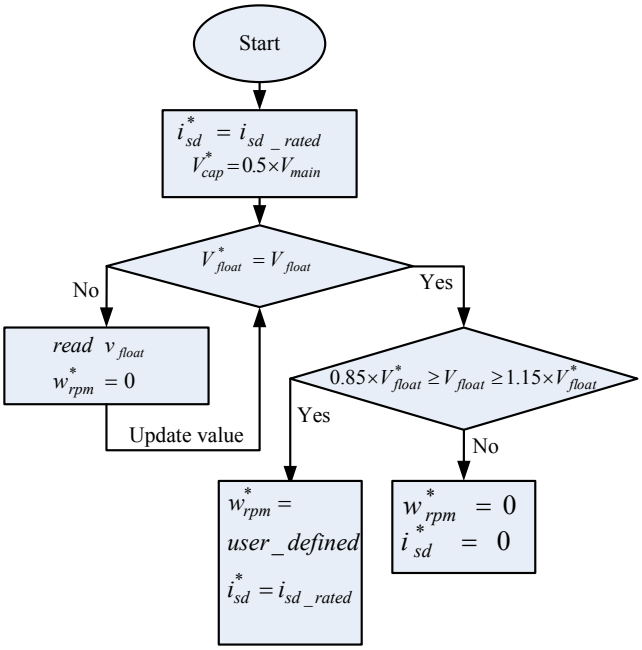

Fig. 18. Floating capacitor charging and protection algorithm.

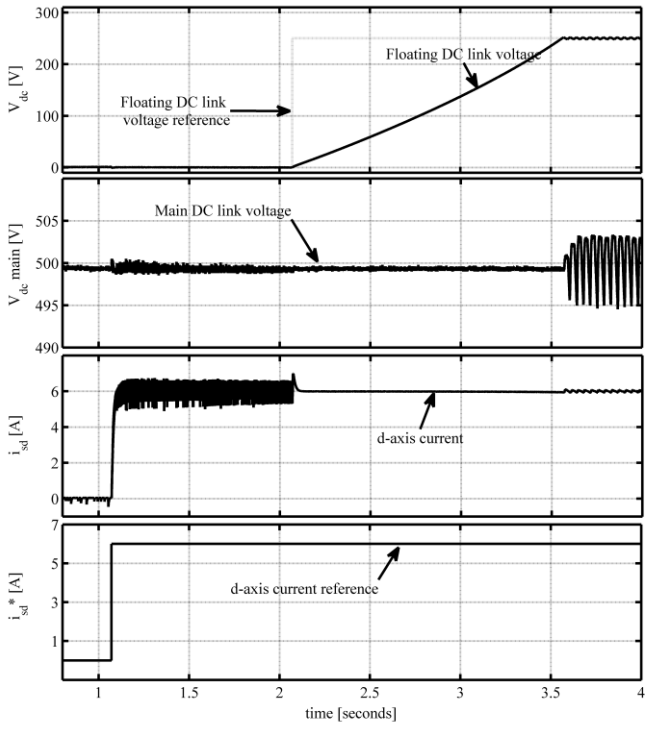

Fig. 19. Initial charging of floating capacitor after machine is magnetized. Top to bottom: floating capacitor voltage and reference, main dc link voltage, d-axis current and d-axis current reference.

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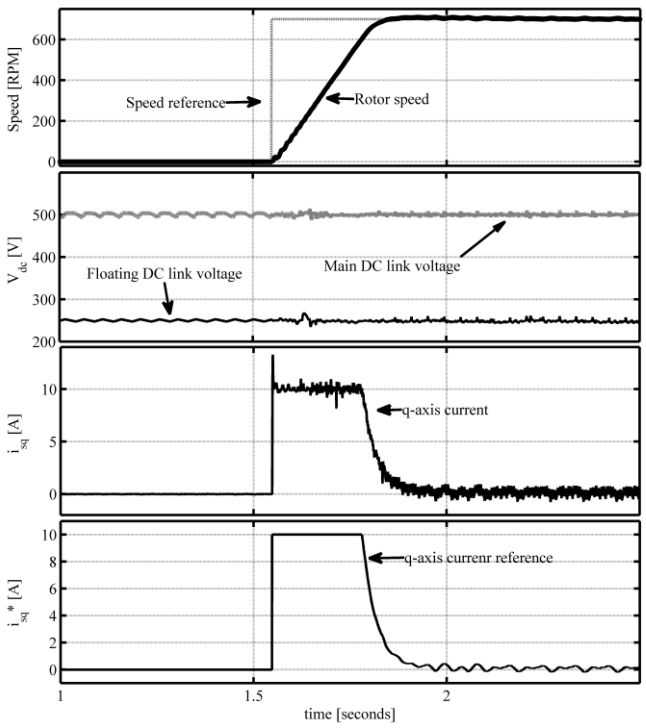

Fig. 20. FOC response of no load speed to a step reference speed command. Top to bottom: rotor speed with reference, floating capacitor and main dc link capacitor voltage , q-axis current and referece q-axis current.

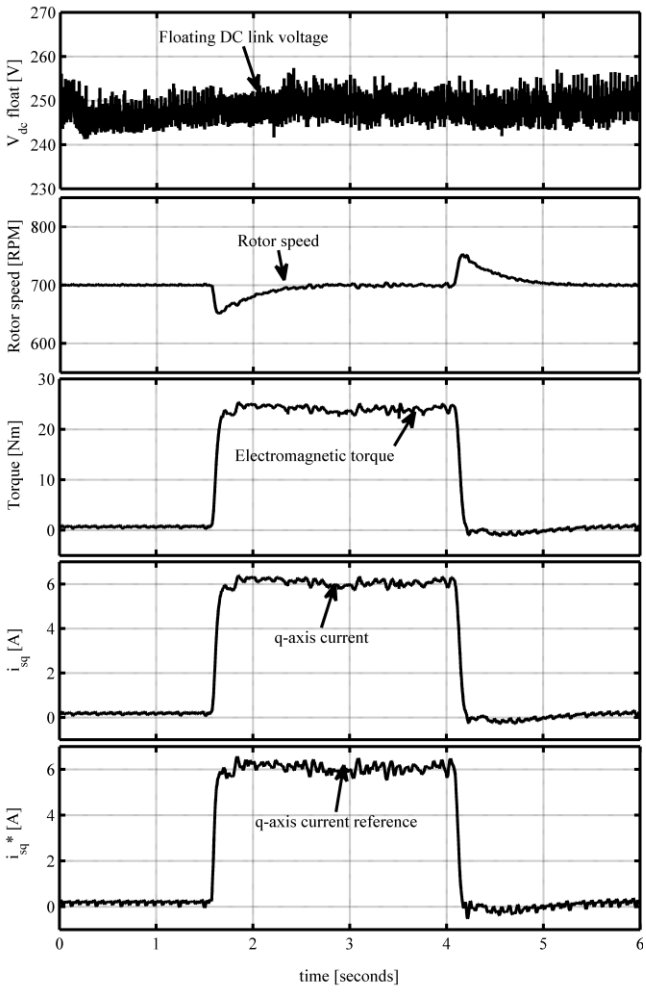

Fig. 21. FOC response to a step load applied after the speed reaches steadystate. Top to bottom: floating capacitor voltage, rotor speed, electromagnetic torque, q-axis current and reference q-axis current.

The charging transient of the capacitor can be made faster with increased d-axis current. It can be seen from the figure that the main DC link voltage fluctuates after the floating capacitor voltage reaches the steady state value, this was due to the charging and discharging of floating capacitor. In this period the rotor was at stand still and the machine was only drawing reactive power to maintain a constant electromagnetic field. In this state, the floating capacitor can be discharged by supplying power to the main supply. After the capacitor voltage reaches steady state, a step demand speed reference of 700 RPM was applied. The response of the controller is shown in Fig. 20. The q-axis current steps up immediately to provide maximum torque to overcome the inertia and holds its value until speed reaches steady state. After the speed reaches steady state, a step demand reference load of 25 Nm was applied at t = 1.5seconds and back to zero at t=4.1seconds. The reference torque current iq* is generated from the speed loop steps up immediately to counter the load torque, as shown in Fig. 21.

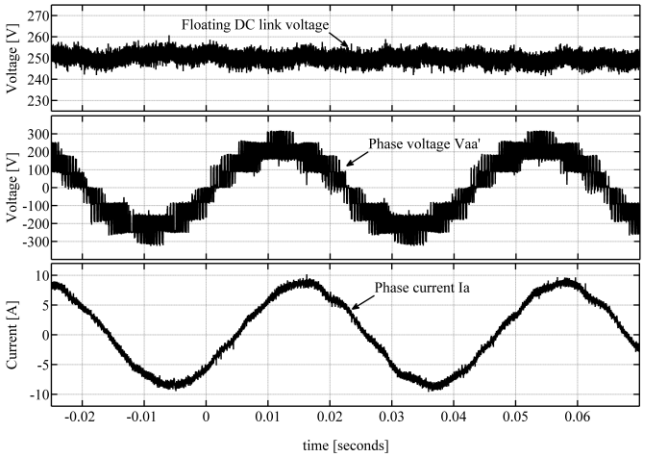

Fig. 22. Phase voltage and current under FOC when machine is loaded. Top to bottom: floating dc link voltage, phase voltage $V_{aa'}$, and phase current I_a.

It can be seen from Fig. 20 and Fig 21 that at no time does the capacitor voltage overcharge or collapse. The capacitor voltage ripple increases at no load as there was a small amount of real power flowing through the system, charging improves with loading condition. Finally the phase voltage, current and floating dc link voltage are shown in Fig. 22 for operation when the machine was loaded.

TABLE III
LOAD AND POWER CONVERTERS PARAMETERS

Induction motor		
Stator resistance	Rs	1.4 Ohm
Rotor resistance	Rr	1.02 Ohm
Stator leakage inductance	Lls	0.0115 H
Rotor leakage inductane	Llr	0.009258 H
Magnetizing inductance	Lm	0.2258 H
Power converter		
Main DC link	Vdc	500 V
Floating DC link	Vf	250 V
Main DC link capacitance	Cm	1250 μF
Floating DC link capacitance	Cf	3250 μF
Gating pulses propagation delay		0.1 – 0.2 μs
Onboard Deadtime	Dt	4 - 4.1 μs
Snubber capacitance	Cs	0.7 nf
Output common mode inductance	Lo	5 μH

IV. CONCLUSIONS

A motor drive using open stator winding induction machine and a dual bridge inverter topology with a floating capacitor bridge has been analyzed and practical results are demonstrated. The proposed system charges the floating bridge capacitor to a ratio of 2:1 with respect to main bridge DC link voltage amplitude. This particular DC link voltage ratio allows the converter to achieve multi-level output voltage waveform. The floating DC link voltage is kept at a constant voltage by the means of charging and discharging the floating bridge capacitor. This is achieved by selecting between the charging and discharging redundant states of the converter. A modified space vector modulation strategy is adopted to eliminate the unwanted voltage levels during the dead-time intervals, thus improved the waveform quality for this floating bridge topology. An open loop v/f control drive was implemented to validate the performance of the capacitor control. Finally, the dynamic performance of the proposed system was evaluated using a close loop field oriented controlled motor drive, the results showed that the proposed topology achieves multi-level output voltage waveforms. The results demonstrate that this topology has potential for applications where size, weight, losses and redundancy are important, for example in aerospace, EV or HEV motor drives.

V. REFERENCES

[1] P. Wheeler, L. Xu, L. Meng Yeong, L. Empringham, C. Klumpner, and J. Clare, "A review of Multi-level Matrix Converter topologies," *IET Conf. on Power Electron., Machines and Drives PEMD*, pp. 286-290, 2008.

[2] J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, pp. 724-738, 2002.

[3] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.,* vol. 57, pp. 2219-2230, 2010.

[4] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A Survey on Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.,* vol. 57, pp. 2197-2206, 2010.

[5] D. Janik, T. Kosan, P. Kamenicky, and Z. Peroutka, "Universal precharging method for dc-link and flying capacitors of four-level Flying Capacitor Converter," *IEEE Conf. on Ind. Electron. Soc. IECON*, pp. 6322-6327, 2013.

[6] E. C. dos Santos, F. Gulpinar, and E. R. C. da Silva, "Flying capacitor four-level H-Bridge converter," *Power and Energy Conf. at Illinois PECI*, pp. 1-6, 2014.

[7] E. Levi, "Multiphase Electric Machines for Variable-Speed Applications," *IEEE Trans. Ind. Electron.*, vol. 55, pp. 1893-1909, 2008.

[8] S. Kouro, J. Rodriguez, W. Bin, S. Bernet, and M. Perez, "Powering the Future of Industry: High-Power Adjustable Speed Drive Topologies," *IEEE Industry App. Mag.*, vol. 18, pp. 26-39, 2012.

[9] F. Betin, G. A. Capolino, D. Casadei, B. Kawkabani, R. I. Bojoi, L. Harnefors*, et al.*, "Trends in Electrical Machines Control: Samples for Classical, Sensorless, and Fault-Tolerant Techniques," *IEEE Ind. Electron. Mag.*, vol. 8, pp. 43-55, 2014.

[10] F. Meinguet, N. Ngac-Ky, P. Sandulescu, X. Kestelyn, and E. Semail, "Fault-tolerant operation of an open-end winding five-phase PMSM drive with inverter faults," *IEEE Conf. on Ind. Electron. Soc. IECON*, pp. 5191-5196, 2013.

[11] N. Ertugrul, W. Soong, G. Dostal, and D. Saxon, "Fault tolerant motor drive system with redundancy for critical applications," *IEEE Power Electron. Spec. Conf. PESC*, pp. 1457-1462 vol.3, 2002.

[12] O. A. Taha and M. Pacas, "Hardware implementation of balance control for three-phase grid connection 5-level Cascaded H-Bridge converter using DSP," *IEEE Int. Symp. Ind. Electron. ISIE*, pp. 1366-1371, 2014.

[13] S. Jae Hyeong, C. Chang-Ho, and H. Dong-Seok, "A new simplified space-vector PWM method for three-level inverters," *IEEE Trans. Power Electron.*, vol. 16, pp. 545-550, 2001.

[14] B. A. Welchko, T. A. Lipo, T. M. Jahns, and S. E. Schulz, "Fault tolerant three-phase AC motor drive topologies: a comparison of features, cost, and limitations," *IEEE Trans. Power Electron.*, vol. 19, pp. 1108-1116, 2004.

[15] N. Bodo, M. Jones, and E. Levi, "PWM techniques for an open-end winding fivephase drive with a single DC source supply," *IEEE Conf. on Ind. Electron. Soc. IECON*, pp. 3641-3646, 2012.

[16] E. Levi, M. Jones, and W. Satiawan, "A multiphase dual-inverter supplied drive structure for electric and hybrid electric vehicles," *IEEE Vehicle Power and Prop. Conf. VPPC*, pp. 1-7*,* 2010.

[17] K. Ramachandrasekhar, S. Mohan, and S. Srinivas, "An improved PWM for a dual two-level inverter fed open-end winding induction motor drive," *Int. Conf. on Electrical Machines ICEM*, pp. 1-6*,* 2010.

[18] E. G. Shivakumar, K. Gopakumar, S. K. Sinha, A. Pittet, and V. T. Ranganathan, "Space vector PWM control of dual inverter fed open-end winding induction motor drive," *IEEE Applied Power Electron. Conf. and Expo. APEC*, pp. 399-405 vol.1, 2001.

[19] V. T. Somasekhar, K. Gopakumar, A. Pittet, and V. T. Ranganathan, "A novel PWM inverter switching strategy for a dual two-level inverter fed open-end winding induction motor drive," *IEEE Int. Conf. on Power Electron. and Drive Systems Proc.*, pp. 196-202 vol.1. , 2001

[20] Y. Zhao and T. A. Lipo, "Space vector PWM control of dual three-phase induction machine using vector space decomposition," *IEEE Trans. Industry App.*, vol. 31, pp. 1100-1109, 1995.

[21] M. R. Baiju, K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Trans. Power Electron.*, vol. 19, pp. 794-805, 2004.

[22] J. Kalaiselvi, K. R. C. Sekhar, and S. Srinivas, "Common mode voltage elimination PWMs for a dual two-level VSI with single inverter switching," *IEEE Int. Symp. Ind. Electron. ISIE*, pp. 234-239, 2012.

[23] G. Grandi, C. Rossi, A. Lega, and D. Casadei, "Multilevel Operation of a Dual Two-Level Inverter with Power Balancing Capability," *IEEE Industry App. Conf. IAS*, pp. 603-610, 2006.

[24] G. Grandi, C. Rossi, A. Lega, and D. Casadei, "Power balancing of a multilevel converter with two insulated supplies for three-phase six-wire loads," *European Conf. on Power Electron. and App.*, pp. 10 pp.-P.10, 2005.

[25] G. Grandi and D. Ostojic, "Dual inverter space vector modulation with power balancing capability," *IEEE EUROCON*, pp. 721-728, 2009.

[26] D. Casadei, G. Grandi, A. Lega, C. Rossi, and L. Zarri, "Switching Technique for Dual-Two level Inverter Supplied by Two Separate Sources," *IEEE Applied Power Electron. Conf. and Expo. APEC*, pp. 1522-1528, 2007.

[27] D. Casadei, G. Grandi, A. Lega, and C. Rossi, "Multilevel Operation and Input Power Balancing for a Dual Two-Level Inverter with Insulated DC Sources," *IEEE Trans. Ind. App.*, vol. 44, pp. 1815-1824, 2008.

[28] K. Junha, J. Jinhwan, and N. Kwanghee, "Dual-inverter control strategy for high-speed operation of EV induction motors," *IEEE Trans. Ind. Electron.*, vol. 51, pp. 312-320, 2004.

[29] R. U. Haque, A. Kowal, J. Ewanchuk, A. Knight, and J. Salmon, "PWM control of a dual inverter drive using an open-ended winding induction motor," *IEEE Applied Power Electron. Conf. and Expo. APEC*, pp. 150-156, 2013.

[30] J. Ewanchuk and J. Salmon, "A Square-wave Controller for a high speed induction motor drive using a three phase floating bridge inverter," *IEEE Energy Conv. Cong. and Expo. ECCE*, pp. 2584-2591, 2010.

[31] J. Ewanchuk, J. Salmon, and C. Chapelsky, "A Method for Supply Voltage Boosting in an Open-Ended Induction Machine Using a Dual Inverter System With a Floating Capacitor Bridge," *IEEE Trans. Power Electron.*, vol. 28, pp. 1348-1357, 2013.

[32] B. A. Welchko, "A double-ended inverter system for the combined propulsion and energy management functions in hybrid vehicles with energy storage," *IEEE Conf. on Ind. Electron. Soc. IECON*, p. 6 pp, 2005.

[33] K. A. Corzine, M. W. Wielebski, F. Z. Peng, and W. Jin, "Control of cascaded multilevel inverters," *IEEE Trans. Power Electron.,* vol. 19, pp. 732-738, 2004.

[34] K. A. Corzine, S. Lu, and T. H. Fikse, "Distributed Control of Hybrid Motor Drives," *IEEE Trans. Power Electron.*, vol. 21, pp. 1374-1384, 2006.

[35] K. A. Corzine and S. Lu, "Comparison of hybrid propulsion drive schemes," *IEEE Electric Ship Techno. Symp.*, pp. 355-362, 2005.

[36] A. Lega, "Multilevel converters: Dual two-level inverter scheme," *Ph.D., department of electrical engineering*, University of Bologna, Bologna, Italy, 2007.
[37] B. V. Reddy and V. T. Somasekhar, "A Dual Inverter Fed Four-Level Open-End Winding Induction Motor Drive With a Nested Rectifier-Inverter," *IEEE Trans. Ind. Info.*, vol. 9, pp. 938-946, 2013.
[38] S. Chowdhury, P. Wheeler, C. Gerada, and S. Lopez Arevalo, "A dual inverter for an open end winding induction motor drive without an isolation transformer," *IEEE Applied Power Electron. Conf. and Expo. APEC*, pp. 283-289, 2015.
[39] S. Chowdhury, P. Wheeler, C. Gerada, and C. Patel, "A dual two-level inverter with a single source for open end winding induction motor drive application," *Euro. Conf. on Power Electron. and App. EPE-ECCE-Europe*, pp. 1-9, 2015.
[40] M. Darijevic, M. Jones, and E. Levi, "An Open-end Winding Four-level Five-phase Drive," *IEEE Trans. Ind. Electron.*, vol. PP, pp. 1-1, 2015.
[41] M. Darijevic, M. Jones, and E. Levi, "Analysis of dead-time effects in a five-phase open-end drive with unequal DC link voltages," *IEEE Conf. on Ind. Electron. Soc. IECON*, pp. 5136-5141, 2013.

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